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Nucleation and growth of Si on Pb monolayer covered Si(111) surfaces

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ABSTRACT

With a scanning tunneling microscope (STM), we study the initial stage of nucleation and growth of Si on Pb monolayer covered Si(111) surfaces. The Pb monolayer can work as a good surfactant for growth of smooth Si thin films on the Si(111) substrate. We have found that nucleation of two-dimensional (2D) Pb-covered Si islands occurs only when the substrate temperature is high enough and the Si deposition coverage is above a certain coverage. At low deposition coverages or low substrate temperatures, deposited Si atoms tend to self-assemble into a certain type of Si atomic wires, which are immobile and stable against annealing to $\sim 200^\circ\text{C}$. The Si atomic wires always appear as a double bright-line structure with a separation of $\sim 9\text{ \AA}$ between the two lines. After annealing to $\sim 200^\circ\text{C}$ for a period of time, some sections of Si atomic wires may decompose, meanwhile the existing 2D Pb-covered Si islands grow laterally in size. The self-assembly of Si atomic wires indicate that single Si adatoms are mobile at the Pb-covered Si(111) surface even at room temperature. Further study of this system may reveal the detailed atomic mechanism in surfactant-mediated epitaxy.

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1. Introduction

Epitaxial growth of flat and high-quality thin films is technologically important for fabrication of many advanced materials and devices. Understanding the fundamental nucleation and growth mechanism is also of great scientific interest. Growth of islands of 3D character is common, especially in heteroepitaxy, which has become a major obstacle for engineering specific thin film structures. A growth method, called surfactant-mediated epitaxy (SME), was introduced in late 1980's [1–3]. With SME, layer-by-layer growth can be achieved by deposition of a surfactant layer on the substrate of material “A” before growing material “B”. With the appropriate choice of this third material, the surfactant layer floats on top of the growing film during the deposition of material “B”. That means the deposited atoms will eventually exchange with the surfactant atoms to get buried underneath the surfactant layer. So far, many SME systems have been reported to suppress 3D island growth [1–28]. However, how the surfactant improves the growth process remains unclear.

Growth of high-quality SiGe thin films on Si substrates is technologically important, as current IC industry mainly uses Si-based materials. Evans et al. reported high-quality homoepitaxial growth on Si(111) surfaces at temperature around 300°C using a monolayer of Pb as the surfactant [25]. They have shown that the Pb coverage should

be exactly 1 ML (1 ML = 1 monolayer = 7.84×10^{14} atoms/cm²). Excess or deficiency of Pb atoms can cause defects in the grown Si thin films. Later, Hwang et al. also reported that nearly perfect layer-by-layer growth for Ge heteroepitaxy on Si(111) at temperatures below 200°C using a monolayer of Pb as the surfactant [26]. These studies suggest very similar growth behavior for both systems. An important implication is that the Pb monolayer may serve as a good surfactant for growing high-quality SiGe thin films on the Si(111) substrate at low temperatures. One may be able to grow SiGe superstructures with very sharp interfaces due to low interfacial diffusion at low temperatures. It might also be possible to control the SiGe superstructure and the doping concentration at atomic layer or sub-atomic layer level [27,28]. Another advantage for using the Pb monolayer as the surfactant is that Pb has a very low solubility in bulk Si and Ge [29]. Thus one does not need to worry about the problem of intermixing of surfactant atoms in the thin films, which might affect the electronic properties of the films.

Hwang et al. have carefully studied nucleation and growth of Ge on the Pb monolayer covered Si(111) surface [in short, Pb/Si(111)], which exhibits many novel behaviors that cannot be explained by the rate-equation based nucleation theories [30–32]. In that system, the deposited Ge atoms are very mobile at the Pb/Si(111) surface at room temperature and can diffuse a very long distance to form a nucleus or to get incorporated into existing island edges. At the same growth temperature and the same flux, the number density of two-dimensional (2D) Ge islands can vary with the Ge coverage by three orders of magnitude. It has been found that the nucleation and growth processes are not rate limited by surface diffusion of Ge atoms and that these processes require overcoming certain energy barriers. Hwang et al. suggested that the nucleation and growth processes

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were rate limited by the exchange reactions of Ge with the Pb layer [30,31] and they concluded that the growth system of Ge on Pb/Si(111) belonged to the “reaction-limited” regime, contrary to the “diffusion-limited” regime assumed in the traditional mean-field theory of nucleation.

There are several other interesting observations for the nucleation and growth of Ge on the Pb/Si(111) surface reported by Hwang et al. [30–32]. It was found that there was a threshold deposition coverage for nucleation of Ge islands to occur. This coverage was estimated to be 0.14 ML at room temperature and it decreased with increasing substrate temperature. Below the threshold coverage, all deposited Ge atoms were much too mobile for STM to image and no deposited material was observed. Above the threshold coverage, 2D Pb-covered Ge islands were seen, but it was estimated that, at room temperature, there was still ~0.09 ML of deposited Ge atoms that could not be seen with STM. It was proposed that those Ge atoms also formed into certain mobile species (probably Ge clusters). Due to certain energy barriers for nucleation into 2D islands and for getting incorporated into existing islands (growth), it was believed that those Ge species remained highly mobile on the surface near room temperature. After annealing, interestingly, growth from existing island edges was seen probably because some mobile Ge species could overcome the energy barriers to get incorporated into the edges. Since the epitaxial growth phenomena of Si on Pb/Si(111) and Ge on Pb/Si(111) are very similar, it would be very interesting to compare the nucleation and growth behaviors of these two systems. As Si atoms are expected to form stronger covalent bonds than Ge atoms on the surface, we might have a chance to image other structures in addition to 2D islands, which can provide important clues for atomic mechanisms in these two SME systems.

At room temperature, there are two phases for monolayer of Pb on Si(111), i.e. the Pb-(1×1) and the so-called “incommensurate” (or Pb-IC) phases [33–36]. Both phases can be used for SME and they are basically an unreconstructed Si(111) substrate with each first-layer Si atom terminated by a Pb atom on the top. In the Pb-(1×1) phase, the Pb atoms are on the T_1 site. In the Pb-IC, each Pb atom is either on the T_1 site or slightly displaced from the ideal T_1 site to form trimer domains [34–36]. Another difference between the IC and the Pb-(1×1) phases is at the substrate step edges. It has been found that gentle annealing causes gradual Pb desorption starting from the upper step edges, meanwhile the surface structure on flat terraces gradually changes from the Pb-IC phase into the Pb-(1×1) phase [26,30–32]. It has also been shown that deposited Ge atoms can attach to the Si(111) substrate step edges on the Pb-IC phase [26], but almost no Ge attachment to the substrate step edges was seen on the Pb-(1×1) phase at room temperature [30–32]. These observations suggest that there is a deficiency in Pb atoms at the upper substrate step edges on the Pb-(1×1) phase.

As illustrated in the side-view atomic model shown in Fig. 1, the Pb coverages on flat terraces are the same for both Pb-IC and Pb-(1×1) phases. This is consistent with previous observations that the Pb covered Ge islands nucleated on both the Pb-IC and the Pb-(1×1) phases have very similar surface structures [26,30–32], suggesting a very similar nature in the atomic structure of these two phases. In the Pb-IC phase, the upper step edges are terminated with Pb atom, which may facilitate the attachment of Si or Ge atoms to the edges through the exchange with the Pb atoms. On the other hand, no Pb atoms are present at the upper step edges in the Pb-(1×1) phase and thus certain Si reconstruction might be formed at the edges to reduce the number of dangling bonds, which may result in higher energy barriers for attachment of Si or Ge atoms.

The Pb-IC phase is more favorable for growing high-quality thin films, because step-flow (growth of thin films from substrate step edges) can occur at appropriate temperatures. The Pb-(1×1) phase is more favorable for the study of nucleation and growth behaviors at sub-monolayer coverages, because nucleation and growth occur only

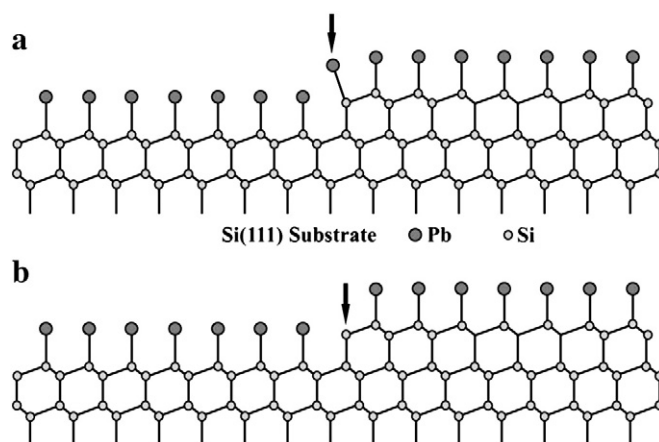


Fig. 1. Atomic models for the Pb-covered Si(111) surfaces. (a) In the so-called Pb-IC phase, the upper step edges are terminated with Pb atoms. On flat terraces, the Pb atoms are either on the T_1 site or slightly displaced from the T_1 site (not illustrated). (b) In the Pb-(1×1) phase, Pb atoms have desorbed from the upper step edges. The Pb atoms are on the T_1 site on flat terraces. Arrows indicate the step edges.

on the flat substrate terraces and the substrate step edges would not consume deposited atoms, especially in the case that deposited atoms have a very long diffusion length.

In this study, we report the nucleation and growth behavior of Si deposition on the Pb monolayer covered Si(111) surface. In order to observe the processes at early stages, we carry out experiments at relatively low temperatures in comparison with typical epitaxial growth temperatures. This is because processes having low activation energies cannot be seen at high temperatures because they are much too fast for STM imaging. In addition to 2D Pb-covered Si islands, we find self-assembly of Si atomic wires, especially when the deposition coverage or the deposition temperature is not high enough. The self-assembly of Si atomic wires indicates high mobility of deposited Si atoms on the Pb-covered Si(111) surface. Our observations also show that nucleation and growth of 2D islands and self-assembly of Si atomic wires are all reaction-limited.

2. Experimental

The experiments are carried out using a homemade scanning tunneling microscope (STM) in an ultra-high vacuum (UHV) chamber with a base pressure of $\sim 1.0 \times 10^{-10}$ Torr. A P-doped Si(111) sample (resistivity 0.05–0.1 Ω -cm) is used. The sample is resistively heated inside the UHV chamber up to ~ 1200 °C for a few seconds to clean the sample surface. After that, the temperature is decreased to ~ 900 °C and stays for about one minute, and then the sample is cooled down to room temperature slowly at a rate of about 1 °C/s. Typically, we can obtain a clean Si(111)-(7×7) surface, as confirmed by a low energy electron diffraction (LEED) instrument. Slightly more than 1 ML of Pb (99.999% purity) atoms are deposited onto the Si(111)-(7×7) surface at room temperature. The sample is then annealed at ~ 500 °C for ~ 1 s followed by a gentle annealing at ~ 300 °C for ~ 5 s. During the annealing, the deposited Pb atoms destroy the Si(111)-(7×7) reconstruction and an incommensurate (IC) phase is formed, as observed with satellite spots around the $\{1/3, 1/3\}$ positions in the LEED pattern [33]. It is a bulk-terminated Si(111) substrate covered with 1 ML of Pb atoms, as determined with Rutherford backscattering [25,33,37,38]. We note that additional Pb atoms over one monolayer have been desorbed from the surface during the thermal treatment. This can be achieved easily thanks to the rapid increase in the desorption rate at Pb coverages just higher than 1 ML [25,33]. Subsequent gentle annealing of the sample at ~ 300 °C gradually changes the Pb-IC phase to a Pb-(1×1) phase, as monitored by LEED. The procedure is very similar to that in previous studies of Ge deposition on the Pb

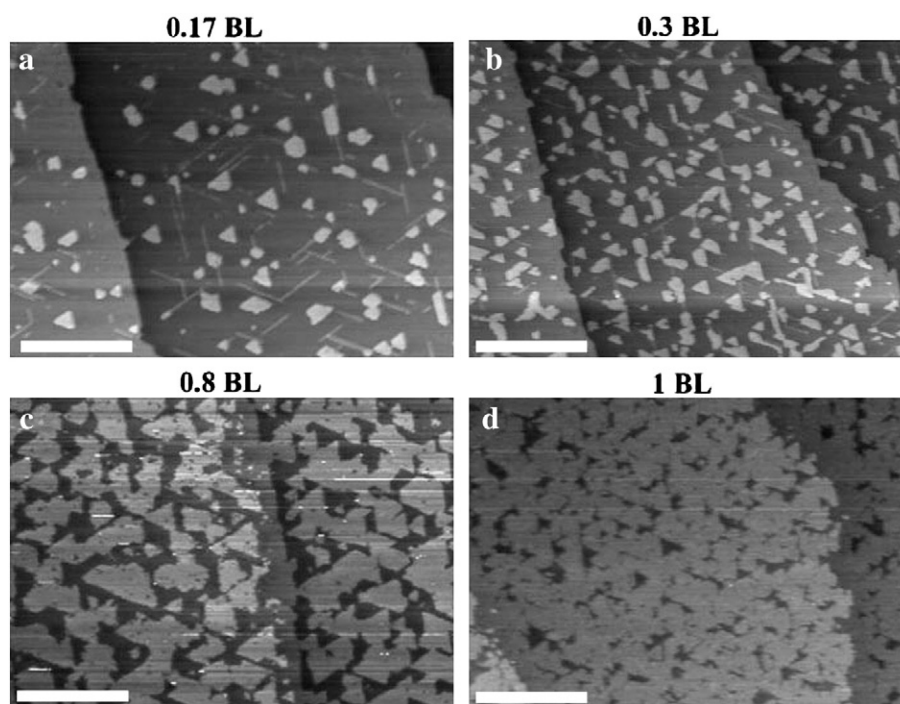


Fig. 2. STM images of surface morphology after deposition of Si atoms on the Pb-1C phase with Si coverage of (a) 0.17 BL (b) 0.3 BL (c) 0.8 BL and (d) 1 BL. The deposition temperature is 150 °C and the deposition flux is 0.17 BL/min. Scale bar length is 100 nm.

monolayer covered Si(111) surface [26,30–36]. We note that, for the Pb-(1 × 1) phase, small regions of the low-coverage (~1/3 ML) Si(111)- $\sqrt{3} \times \sqrt{3}$ -Pb phase [33] may be present at the upper

substrate step edges and the areas depend on how much Pb has been desorbed from the surface. In our Pb-(1 × 1) samples, the $\sqrt{3} \times \sqrt{3}$ areas are too small to produce any detectable LEED pattern.

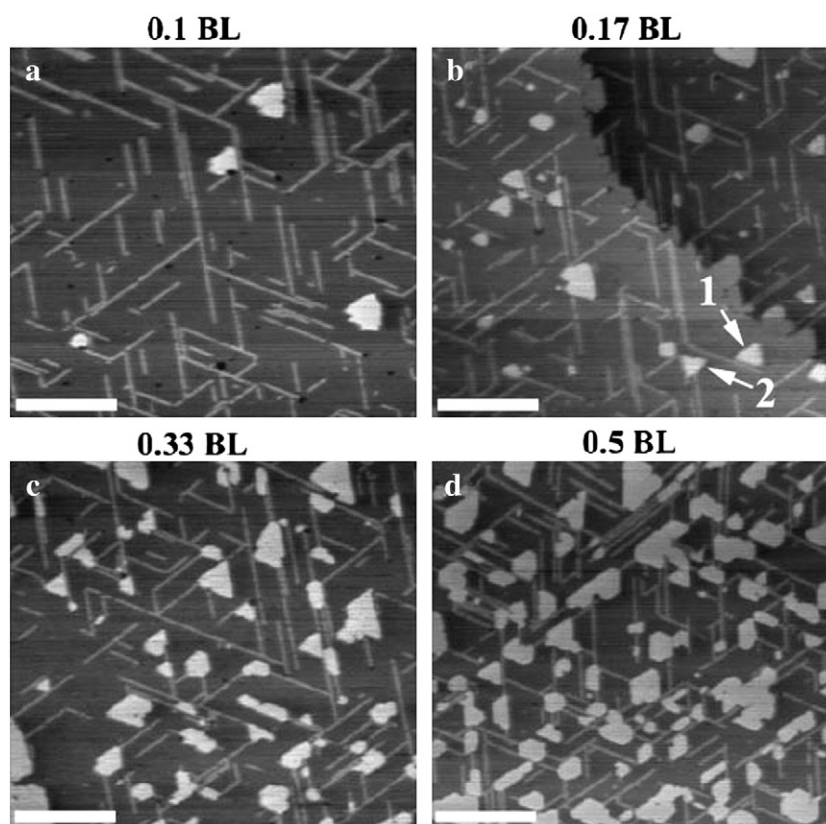


Fig. 3. STM images of surface morphology taken after Si deposition on the Pb-(1 × 1) phase at 150 °C with a flux of 0.17 BL/min. The deposition coverage is indicated on the top of each image. In (b), arrow 1 indicates a Pb-covered Si island with the right stacking sequence; while arrow 2 indicates another Pb-covered Si island with the wrong stacking sequence, which exhibits as a triangle 60° rotated relative to the former one. From the shape of the nucleated 2D islands, we can conclude that most of them have the right stacking sequence. Scale bar length is 50 nm.

Si atoms are evaporated from a Knudsen cell and deposited onto the Pb-covered surface. The sample is then transferred to the STM stage for imaging. The Si deposition flux is calibrated by how much time it takes (with continuous deposition) to fill up a whole bilayer (1 BL = 2 ML), as determined later by the STM. To prepare a sample with a different deposition condition, such as a different deposition coverage or a different deposition temperature, the sample is usually annealed to a temperature above 900 °C to desorb all Pb atoms from the surface. A clean Si(111)-(7×7) surface is obtained after the sample is cooled down to room temperature. A new Pb-covered surface is prepared and then a new Si deposition is carried out on the surface, as the procedure described above. To increase the Si deposition coverage, we always prepare a new sample with a longer deposition time. We do not add Si to a sample to increase the Si coverage.

STM data acquisition is usually initiated at least an hour after Si deposition. All STM images presented here are taken at room temperature and in the constant current mode. Unless the tunneling condition is otherwise specified, the sample bias is +2 V and the tunneling current ~50 pA. Under such a condition, the Pb-covered Si (111) surface appears flat with little corrugation [26,30–36].

3. Results

Fig. 2 shows the growth morphology of Si homoepitaxy on the Pb-IC phase at several different deposition coverages. The deposition flux is 0.17 BL/min and the sample temperature is 150 °C. At the coverage of 0.17 BL, a number of 2D islands have appeared on flat terraces (Fig. 2a). The islands are small and compact in shape and tend to be faceted with edges parallel with the substrate <011> directions. The surface of 2D islands appears flat, similar to that of the Pb-covered Si(111) surface before Si deposition. High-resolution images of the surface on the islands also reveal the Pb-IC phase, thus we conclude that the 2D islands are also covered with one monolayer of Pb. The exchange processes between deposited Si and Pb overlayer have occurred. Besides the 2D Pb-covered Si islands, interestingly, one-dimensional (1D) Si atomic wires are found to coexist with the Pb-covered Si islands, as seen in Fig. 2a. These wires lie along one of the three equivalent <011> crystalline directions. Since the substrate has a three-fold symmetry, there are three different orientations for the Si atomic wires. The number density of Si atomic wires decreases with increasing Si coverage, meanwhile the average size of 2D islands increases, as shown in Fig. 2b and c. Only a small number of Si atomic wires can be observed in Fig. 2b and they are hardly seen in Fig. 2c. At the coverage of ~1 BL (Fig. 2d), the 2D islands grow laterally and coalesce into the first bilayer thin film. Clearly, the Pb-mediated Si homoepitaxy follows the layer-by-layer growth mode, i.e., no 2D islands of the second bilayer appear before completion of the first bilayer. This is very similar to the case of Ge epitaxy on the Pb-IC phase at room temperature reported earlier [26].

When Si atoms are deposited on the 1×1 phase at the same substrate temperature (150 °C), a much higher number density of Si atomic wires are present (Fig. 3). With a Si deposition coverage of 0.1 BL, most deposited Si atoms are in the form of 1D Si atomic wires (Fig. 3a), and only a small number of 2D islands are seen. The surface of the islands also appears flat, indicating that they are Pb-covered Si islands. With a higher Si deposition coverage of 0.17 BL (Fig. 3b), the number density of 2D islands increases compared with the case in Fig. 3a and many 2D islands are very small in their lateral size. When Si deposition coverage increases to 0.33 BL (Fig. 3c), we see a much higher number density of the 2D islands and the average size increases relative to the case in Fig. 3b. In addition, the number density of Si atomic wires in Fig. 3 is significantly higher than the case on the Pb-IC phase as shown in Fig. 2. These results seem to indicate that the slight deficiency in the surface Pb atoms at the substrate step edges favors formation of 1D Si atomic wires over formation of 2D

islands. With an even higher Si deposition coverage of 0.5 BL, the number density and the average size of 2D islands increases further, as shown in Fig. 3d. Clearly, the ratio of deposited Si atoms in the form of 2D islands to those in the form of atomic wires increases with increasing deposition coverage.

Each of the Si atomic wires seen in the low-resolution images, as shown in Figs. 2 and 3, actually appears as a double-line structure in the high-resolution images. Fig. 4a shows a high-resolution image of a Si atomic wire, which appears as a pair of bright lines. The line profile shows that the pair is separated by ~9 Å and the bright lines are about ~1.5 Å higher than the Pb-(1×1) region (Fig. 4b). We note that the apparent height varies from 1.5 to 2.5 Å depending on the sample bias. The wire appears to have a periodicity of 3.84 Å along the wire direction, same as the periodicity in the surrounding Pb-(1×1) region. The Si atomic wires are very stable and immobile at room temperature. The self-assembly of 1D Si atomic wires indicates that Si atoms are very mobile after deposition on the surface.

The average length of Si atomic wires increases with increasing deposition coverage and increasing substrate temperature. Fig. 5 shows STM images of the growth morphology after Si deposition on the Pb-(1×1) surface at room temperature. The Si deposition coverage is 0.014 BL, 0.085 BL, and 0.13 BL for Fig. 5a, b, and c, respectively. At such a low temperature, the number density of Si atomic wire is high and the average length is short, as compared with the case in Fig. 3. In Fig. 5a, short Si atomic wires with the average length of ~2.4 nm are seen. The average length increases to ~4.5 nm as the Si coverage increases to 0.085 BL (Fig. 5b). When the Si coverage increases to 0.13 BL, small 2D islands are seen near the end of some Si

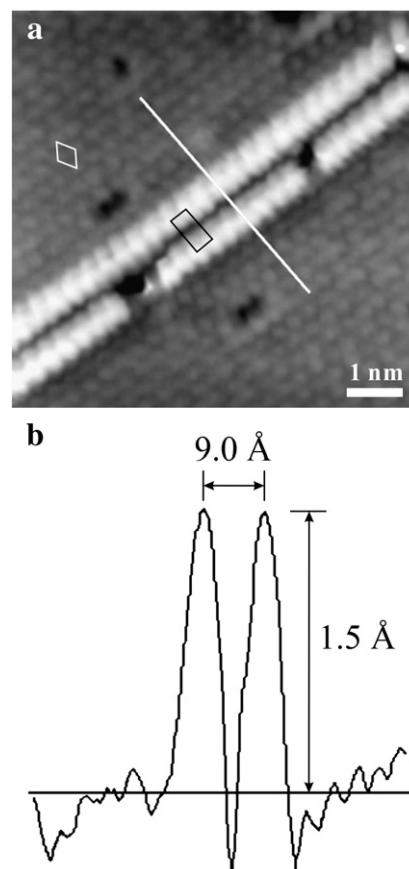


Fig. 4. (a) High-resolution STM image of Si atomic wires taken at the sample bias of +0.79 V and the tunneling current of 0.16 nA. Surrounding the pair structure is the Pb-(1×1) structure (a white unit cell is outlined) with a separation of ~3.84 Å between neighboring Pb atoms. A unit cell of the Si atomic wire is also outlined. (b) Height profile across a Si atomic wire along the white line in (a).

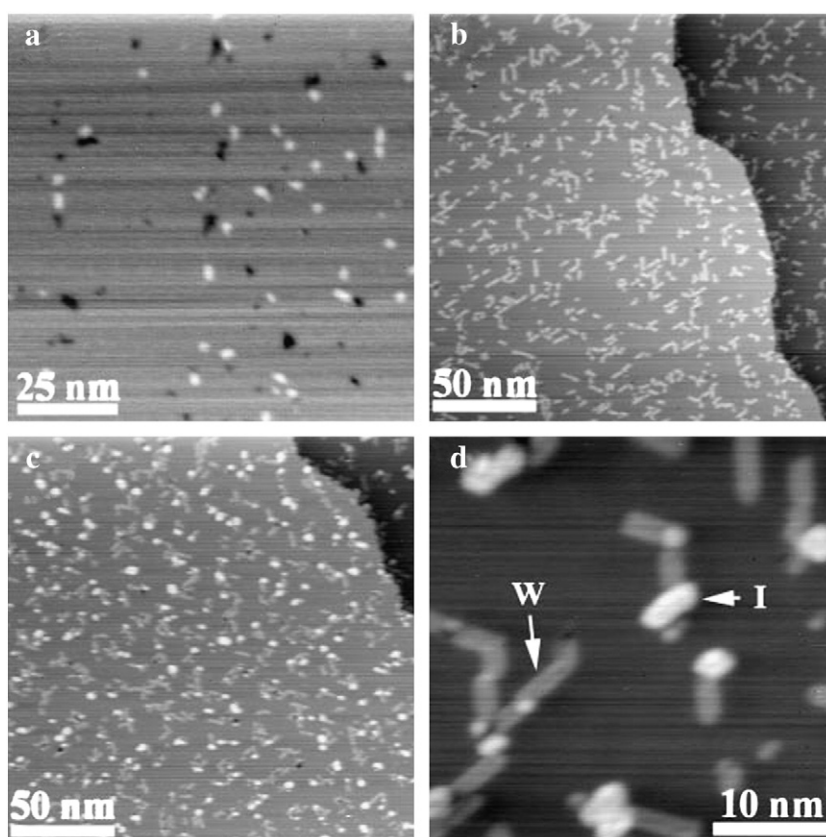


Fig. 5. STM images of surface morphology taken after Si deposition on the Pb-(1 × 1) phase at a coverage of (a) 0.014 BL; (b) 0.085 BL; (c) and (d) 0.13 BL Si atoms. The deposition is carried out at RT with a flux $F = 0.17$ BL/min. (d) is a higher resolution image taken on the same sample as in (c). A nucleated 2D island is indicated with “I” and a Si atomic wire is indicated with “W”.

atomic wires (Fig. 5c and d). A higher resolution image shown in Fig. 5d reveals the double-line feature of the Si atomic wires.

Fig. 6 shows the surface morphology of Si deposition at three different deposition temperatures. The Si deposition coverage is 0.085 BL for these three experiments. At room temperature, all deposited Si atoms are in the form of short Si atomic wires (Fig. 6a). When the temperature increases to 100 °C, the average length of Si wires significantly increases and the number density decreases (Fig. 6b). In addition, a low number density of small 2D islands can be seen, as indicated by arrows in Fig. 6b. When the substrate temperature increases to 200 °C, a very low number density of large 2D islands is seen (Fig. 6c), indicating that most deposited Si atoms form into 2D islands. This indicates that the Si atomic wires are metastable and the 2D Pb-covered Si islands are the most stable structure. Notice that some Si atomic wires still can be seen in Fig. 6c.

Fig. 7a shows a STM image of a surface after Si deposition of 0.1 BL at 150 °C. Most Si atoms are in the form of Si atom wires, but a few 2D islands are also present. After annealing this sample at 200 °C for 15 min, the image taken at the same area (Fig. 7b) shows that some segments of Si atomic wires disappear while the original 2D islands grow laterally. It clearly shows that the growth of 2D islands is at the expense of Si atomic wires. Surprisingly, most Si atomic wires remain after the annealing, suggesting the high stability of Si atomic wires against heating.

4. Discussion

4.1. Si atomic wires

The Si atomic wires presented here are much smaller than the Si nanorods or Si nanowires that have been reported in the literature. We still do not know the atomic structure of Si atomic wires at this

moment. From the high-resolution image of the atomic wire shown in Fig. 4a, one may consider an intuitive (maybe naïve) model: double Si atomic lines with each bright spot as a Si atom on top of the Pb overlayer. Concerning this model, we may want to ask the following questions. Why do the Si lines always appear in pairs? What keeps the separation of the double lines fixed at ~9 Å? How do the Si atoms on one line know the presence of the other Si lines 9 Å away? It is known that the Si–Pb bonds are weak, then why are many Si lines stable against annealing to ~200 °C?

Even though we have resolved the unit cell of the Si atomic wires, we do not know their atomic structure nor the number of Si atoms in each unit cell. However, we still can reach some preliminary conclusions based on our analysis of the STM images. The double-line feature always appears brighter than the Pb layer from –2 V to +2 V, suggesting that the Si atomic wires are geometrically higher than the Pb layer. Each bright spot of the atomic wire seen in the STM image (Fig. 4a) may be a Si atom or a small Si structure on the top. The line profile across the Si wires as shown in Fig. 4b indicates that the region between the double lines is lower than the Pb layer, suggesting that there are no Pb atoms between the double lines. We guess there could be a certain Si structure connecting between the Si line structure on both sides. This would explain why the Si wires always appear with a double-line feature and why the separation of the double lines is fixed at ~9 Å. Also, the good stability of Si atomic wires against annealing to ~200 °C suggests that the Si wires might not be grown on top of the Pb overlayer, rather they probably form strong covalent bonds to the underneath Si substrate directly. That means the height of Si atomic wires might be 5–6 Å above the Si substrate considering the size of a Pb atom (3.5 Å) [33]. There might be a three-dimensional (3D) structure in the Si wires and STM images only reveal the top-layer structure. Further experimental and theoretical studies are needed to resolve the atomic structures of the Si atomic wires.

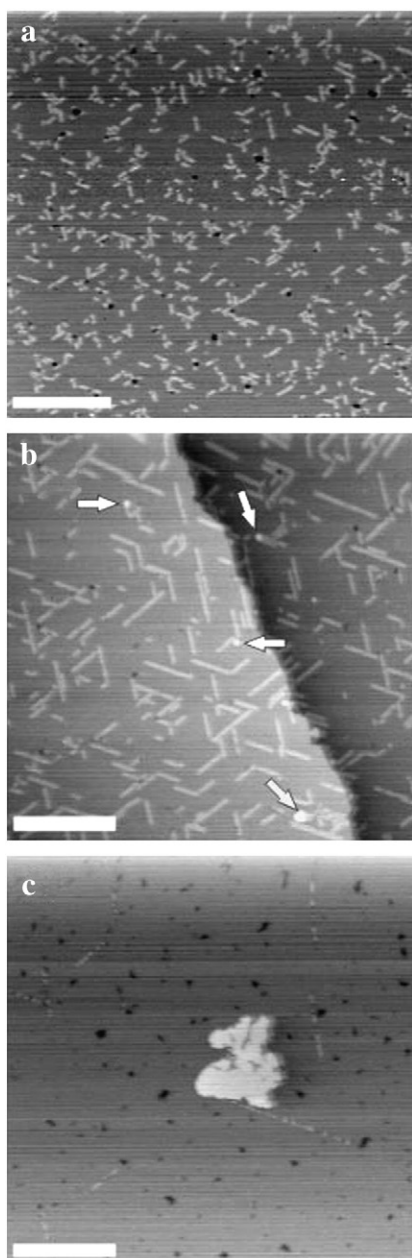


Fig. 6. STM images of the surface morphology after deposition of Si atoms of 0.085 BL on the Pb-(1 × 1) phase at the substrate temperature of (a) RT, (b) 100 °C, (c) 200 °C. The deposition flux is 0.17 BL/min. In (b), some nucleated 2D islands are indicated with arrows. Scale bar length is 50 nm.

4.2. Nucleation and growth of Si on Pb monolayer covered Si(111) surfaces

As shown in Fig. 7, some sections of Si atomic wires disappear after annealing, meanwhile the 2D Pb-covered Si islands enlarge in their lateral sizes. The 2D islands are located at some distance away from the Si atomic wires. It suggests that some sections of the Si atomic wires decompose into certain mobile Si species, which later get incorporated into existing 2D islands. It also indicates that the 2D Pb-covered Si islands are the most stable and the 1D Si atomic wires are metastable structures. Deposited Si atoms will eventually form into 2D islands if the temperature is high enough and the deposition coverage is large enough. On the other hand, Si atomic wires may be formed when the temperature is not high or when the deposition coverage is too low. No nucleation of 2D islands occurs below a certain deposition coverage on the Pb-(1 × 1) phase, which is very similar to

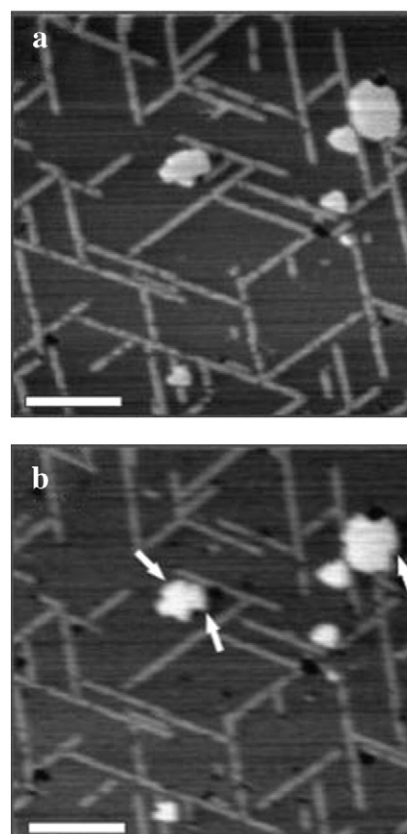


Fig. 7. Morphology change of the surface before and after annealing. (a) Surface morphology after Si deposition of 0.1 BL Si atoms at 150 °C. (b) STM image of the same area after annealing the sample to 200 °C for 15 min. 2D islands grow laterally (indicated with white arrows) and some Si atomic wires disappear. Scale bar length is 50 nm.

previous STM studies of nucleation and growth of Ge on the Pb-(1 × 1) phase [30–32]. It was proposed that the nucleation process was hindered by energy barriers (nucleation barriers) required for mobile Ge species (probably certain types of Ge clusters) to nucleate into a Pb-covered Ge island [30–32]. We believe deposited Si atoms may also need to overcome a similar energy barrier for nucleation into a Pb-covered Si island. Formation of Si atomic wires may require a lower energy barrier than nucleation of 2D islands.

In previous STM studies of nucleation and growth of Ge at Pb/Si(111), there was a coverage (~0.09 ML at room temperature) of deposited Ge atoms that were missing in STM images even 2D Pb-covered Ge islands had been formed [30–32]. It was speculated that those missing Ge atoms were in the form of certain Ge species (probably clusters), which were much too mobile for STM imaging. It was expected that there were also certain energy barriers (growth barriers) for the mobile Ge species to get incorporated into existing 2D islands. Thus those Ge species had arrived at island edges many times but could not lead to the island growth. In this study of nucleation and growth of Si on Pb/Si(111), Si atomic wires are still present even though most deposited Si atoms have formed into 2D islands (Figs. 2a, 3c, 3d, 6c). This also indicates that there are certain energy barriers for the deposited Si atoms to get incorporated into existing Pb-covered Si islands, similar to the case of Ge attachment to existing Pb-covered Ge islands reported earlier [30–32].

Another interesting observation is that no Ge atomic wires, equivalent to the Si atomic wires reported in this work, were seen in previous studies [30–32]. That seems to indicate that Ge atomic wires are not stable at room temperature, thus Ge atoms remain mobile on the surface and cannot be detected with STM. For the case of Si deposition on Pb/Si(111), it seems that deposited Si atoms are

either in the Pb-covered Si islands or in Si atomic wires. We cannot detect any significant coverage of Si atoms that is missing in STM images. However, we still cannot totally rule out a possibility that there remains a very small coverage (<0.01 ML) of mobile Si species at the Pb-covered surface because we do not know the exact number of Si atoms in each unit of the Si atomic wires.

The much lower number density of Si atomic wires for deposition on the Pb-IC phase than on the Pb-(1×1) phase, as seen in Fig. 2a and b, suggests that the energy barriers for incorporation of deposited Si atoms into the existing substrate step edges or island edges on the former phase might be smaller than those on the latter phase. This indicates that presence of Pb atoms at step or island edges facilitates the incorporation of deposited atoms to the edges by lowering the growth barriers. It also suggests that the Pb-IC phase is more favorable than the Pb-(1×1) phase if one would like to grow high-quality SiGe thin films. The step-flow growth mode can be expected to occur on the Pb-IC phase if the deposition temperature is high enough. Evans et al. have found that high quality Si thin films can be grown at a lower temperature on a higher miscut angle Si(111) substrate using the monolayer Pb as the surfactant [25]. We believe this might be related to the step-flow growth mode for Si homoepitaxy on the Pb-IC phase. Even though we have shown that layer-by-layer growth mode can also occur on the Pb-(1×1) phase, there is always a chance for nucleation of 2D islands with a wrong stacking (see island 2 in Fig. 3b). Previous studies of Ge deposition on the Pb-(1×1) phase also indicated a small percentage of nucleated 2D Ge islands with the wrong stacking sequence [32]. Even though flat Si/Ge thin films can be grown on the Pb-(1×1) phase, dislocations or stacking faults may probably be present in these films due to coalescence of 2D islands with different stacking sequences. This may explain the previous observation by Evans et al. that the SME grown Si thin films exhibit stacking faults nucleated at the substrate-film interface when the Pb coverage is less than 1 ML [25].

In several reported SME systems, a high density of small 2D islands was observed after deposition, which was ascribed to a reduced diffusion length of deposited adatoms on surfactant-covered surfaces [9–11,15–18,21]. According to the traditional nucleation theory [39–41], which is in the diffusion-limited regime, a high density of 2D islands implies a reduced surface mobility (or a reduced diffusion length) of adatoms. In fact, it remains a question whether those SME systems are in the diffusion-limited regime or not.

It has been shown that the Pb monolayer is a good surfactant for growth of Si/Ge thin films on Si(111) substrates. On clean Si(111)-(7×7), it has been observed that deposited Si atoms cannot move out of its original 7×7 half cell at room temperature [42,43]. In this study, Si atomic wires are formed and no single Si atoms are observed, indicating that deposited Si atoms are already very mobile at room temperature. The annealing experiments shown in Fig. 7 further confirm good surface diffusion for Si atoms. These observations do not support any model that assumes the suppression of surface diffusion of deposited atoms by the surfactant layer.

4.3. Relation between Si atomic wires and 2D islands

After deposition, Si adatoms may self-assemble into Si atomic wires. One may ask whether there are energy barriers for deposited Si atoms to get incorporated into Si atomic wires. Nucleation of Pb-covered Si islands occurring above a certain deposition coverage as shown in Fig. 5 implies the presence of such energy barriers. If there are no such energy barriers, the Si atomic wires would simply grow longer as the coverage increases. On the other hand, if such energies barriers are present, the coverage of mobile Si species would increase with increasing deposition time. When mobile Si species reaches a certain coverage, nucleation of 2D islands may start to occur, similar to the nucleation of Ge islands at the Pb-covered Si(111) surface above a threshold coverage reported previously [30–32].

5. Conclusions

In this work, we report nucleation and growth behaviors of Si on the Pb monolayer covered Si(111) surface. We have demonstrated the layer-by-layer growth behavior, indicating that Pb monolayer is a good surfactant for Si growth on Si(111). In addition to nucleation of 2D Pb-covered Si islands, we also find the self-assembly of 1D Si atomic wires, especially when the deposition coverage or the deposition temperature is not high enough. That suggests Si atomic wires are metastable structures. The self-assembly of Si atomic wires also indicate that single Si adatoms are mobile at the Pb-covered Si(111) surface even at room temperature. The Si atomic wires always appear as a double straight line structure with a separation of ~ 9 Å between the two lines. The line structure is along a Si substrate direction, so the Si atomic wires exhibit three different orientations. The unit cell of the atomic wires is resolved, but neither the detailed atomic structure nor the number of Si atoms in each unit cell is determined. Further study of Si atomic wires and how Si adatoms self-assemble into Si atomic wires, how deposited Si atoms get incorporated into existing Si atomic wires and existing 2D islands, and how 2D islands are nucleated may reveal the detailed atomic mechanism for nucleation and growth of Si on the Pb-covered Si(111) surface. Our STM study also indicates that the nucleation and growth of 2D islands and self-assembly of Si atomic wires are “reaction-limited”, i.e. these processes require overcoming energy barriers. The observed nucleation and growth behaviors are much more complicated than the pictures assumed in the rate-equation based nucleation theories [39,40]. We believe that further understanding of this growth system may shed light on the fundamental mechanisms in surfactant-mediated epitaxy as well as in semiconductor-on-semiconductor growth systems.

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